This listing of claims will replace all prior versions and listings of claims in the application:

1.   (Canceled)

1   2.   (Currently Amended) A computer implemented method of
2 rasterizing a page in a page description language in a
3 multiprocessor integrated circuit comprising the steps of:
4   interpreting said page in said page description language with
5 a first processor of said multiprocessor integrated circuit;
6   spawning a subtask from said first processor to another of
7 said processors for sorting polygon edges in increasing minimum Y
8 coordinate, wherein each of said other processors is a digital
9 signal processor having an integer multiplier unit; and
10   spawning a subtask from said first processor to another of
11 said processors for detecting a Y coordinate of edge intersection
12 determined to occur between Y coordinates Ytop and Ybottom via
13 successive midpoint approximation by repeatedly
14   calculating a difference in the X coordinates of the
15   respective edges at Ytop and Ybottom are computed by
16
17   x1step = X1 - x1
18   x2step = X2 - x2
19
20   where: x1 and x2 are respective X coordinates of two edges at
21   Ybottom; and X1 and X2 are respective X coordinates of said
22   two edges at Ytop,
23   calculating the X coordinates of the respective edges at
24   Y coordinate Y = (y1+y2)/2 by
25
26   X1 = (x1 + x1step)/2

27          $$\underline{X2 = (x2 + x2step)/2}$$

28

29   setting Ybottom as (Y + Ybottom)/2 if X2 > X1 at Y, and
30   setting Ytop as (Y+Ytop)/2 if X2 < X1, and until a Y
31   coordinate of the intersection point is obtained with a
32   desired accuracy.

3 and 4.   (Canceled)

1   5.   (Currently Amended) ~~The~~ A computer implemented method ~~of~~
2   ~~claim 2,~~ of rasterizing a page in a page description language in a
3   multiprocessor integrated circuit comprising the steps of:
4   interpreting said page in said page description language with
5   a first processor of said multiprocessor integrated circuit,
6   wherein said first processor is a reduced instruction set processor
7   having a floating point computation unit ~~and said method further~~
8   ~~comprising:~~;
9   spawning a subtask from said first processor to another of
10   said processors for sorting polygon edges in increasing minimum Y
11   coordinate; and
12   calculating a Y coordinate of edge intersection employing said
13   floating point calculation unit of said first processor by

14

15          $$Y = (c1-c2)/(b2-b1)$$

16

17   where: a first edge has vertices (X1,Y1) and (X2,Y2) with b1 = X1 -
18   X2 and c1 = X2*Y1 - X1*Y2; and a second edge has vertices (X3,Y3)
19   and (X4,Y4) with b2 = X3 - X4 and c2 = X4*Y3 - X3*Y4.

6 to 10.   (Canceled)

1   11.   (Currently Amended) ~~The~~ A computer implemented method ~~of~~
2   ~~claim 2,~~ of rasterizing a page in a page description language in a
3   multiprocessor integrated circuit, comprising the steps of:
4   interpreting said page in said page description language with
5   a first processor of said multiprocessor integrated circuit,
6   wherein the multiprocessor integrated circuit includes plural other
7   processors ~~and said method further comprising:~~;
8   spawning a subtask from said first processor to another of
9   said processors for sorting polygon edges in increasing minimum Y
10   coordinate;
11   forming a queue of parallel tasks with said first processor;
12   and
13   dispatching a parallel task from said queue to a next
14   available other processor.